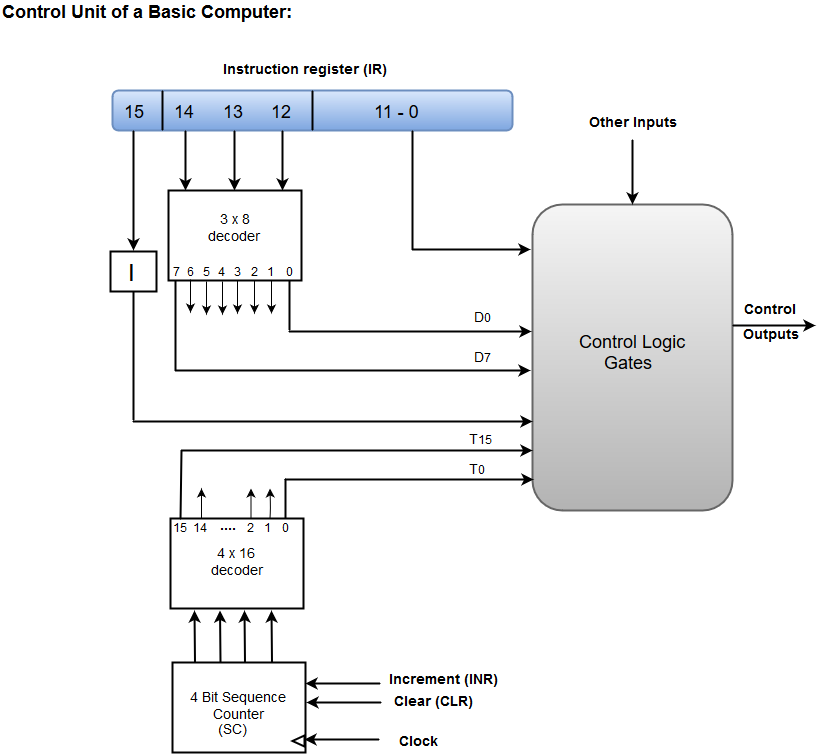
**Timing and Control**

* The timing for all registers is controlled by a master clock generator.
* Clock pulse applied to all flip-flop and registers.
* Clock pulse do not change state of register unless the register is enabled by a control signal.
* After generating control, it provided to multiplexer in common bus, control input in processor register, and micro-operations for the accumulator.
* **Control organization (two types):**
  + **Hardwired control**
    - Implemented with gates, flip-flops, decoders, and other digital circuits.
    - Fast most operation.
    - Hard to modify (i.e. change the components and structure of control).
  + **Microprogrammed Control**
    - Control information stored in a control memory.
    - Control memory programmed to initiate the required sequence of micro-operation.
    - Easy to modify and change. (i.e. re-program according to need).

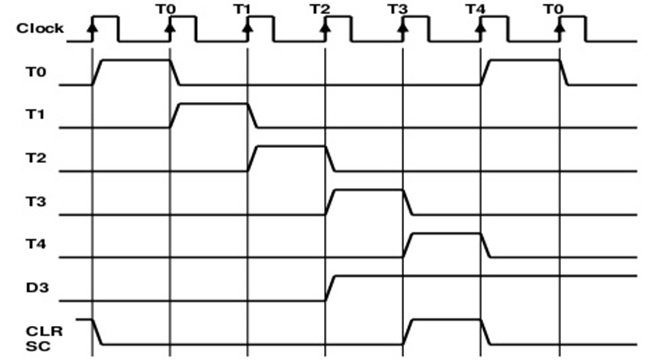


* It consists of two decoders (3x8 decoder and 4x16 decoder), and a sequence counter, and a number of control logic gates.
* Instruction read from memory and stored in IR.
* Instruction register divide in 3-parts: I-bit, Opcode, and bit 0 through 11.
* Opcode (12-14) decoded with 3x8 decoder.
* 8-output decoder are designated by symbol D0 to D7.
* Bit 15 of the instruction is transferred to flip-flop I.
* Bits 0 through 11 are applied to the control logic gates.
* 4-bit sequence counter can count in binary from 0 to 15.
* Output of the counter are decoded into 16-timing signals T0 to T15.
* The sequence counter SC can be incremented or cleared synchronously.
* Incremented from T0 to T15, and once it cleared next active timing signal to be T0. Initially it is cleared.

**Example:**

* Let SC incremented to provide timing signal. T0, T1, T2, T3, T4, ….. in sequence.
* At T4, SC is cleared to 0; if decoder D3 is active.

i.e. D3T4: SC 🡸 0.



* Example explanation:
  + D3T4 = 1, SC 🡸 0.
  + D3 active at end of T2.
  + When T4 active, output of AND gate implements control function D3T4 become active.
  + Applied CLR input of SC.
  + On the next positive clock transition of the counter is cleared to 0.
* SC responds to the positive transition of the clock.
* Initially CLR input of SC is active.
* The first positive transition of the clock clear SC to 0; and activate T0.
* At T0 only trigger those registers whose control connected to T0.
* SC is incremented with every positive clock transition, unless its CLR input is active.
* If CLR is not active, then SC increase from T0 to T15 and back to T0.